Mark schemes

1.

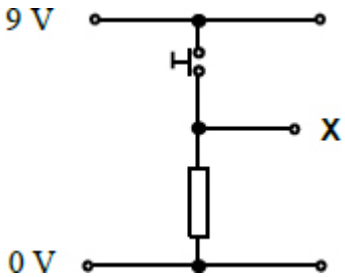
(a)

Inputs			Output
C	B	A	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

*All Q **states** correct for 1 mark*

1

(b)



Correct orientation for resistor & switch ✓

*Correct tap-off point for **X*** ✓

2

(c)

$Q = \overline{(C \cdot A) + (C \cdot B)}$ Two correct brackets ✓

+ with full bar ✓

Allow for 1 mark: $Q = \overline{C \cdot (A + B)}$

2

(d) The gate acts as an inverter ✓

Accept 'NOT' as the function

1

(e) Must be a reason and a consequence for the mark. ✓

eg Uses only one type of logic gate so need to hold less stock

OR

Uses only one chip rather than two so circuit board can be smaller / less power needed / cheaper

Do not allow: Less complex circuit

1

[7]

2.

(a) +ve knee develops at 0.7 V and does not exceed 1.5 V at 30 mA ✓

–ve knee develops at 5.1 V; 5 mA with near vertical drop. Does not exceed – 5.5 V at –30 mA ✓

2

(b) Zener diode provides a reference voltage for non-inverting input ✓

Or

Zener diode provides a stabilised voltage for non-inverting input ✓

Accept combination of the two statements

1

(c) **I = V/R** = 3.9 V / 100 Ω = 39 mA

This is larger than the minimum current to make Zener diode work so the resistor value is fine. ✓

$\mathbf{P = I^2 R} = (39 \times 10^{-3})^2 \times 100 = 0.152$ watts

This is greater than the power rating for the resistor, so is not a suitable power rating for the resistor ✓

Ecf from value of ***I***

2

(d) The reference voltage at the non-inverting input is now smaller ✓

This will cause the output **W** to switch at a lower light intensity than before ✓

2

(e) $Q = \overline{(X + Y)} \cdot W$ ✓

Accept transformations eg

$Q = \overline{X} \cdot \overline{(Y + \overline{W})}$

$Q = \overline{X} \cdot Y \cdot \overline{W}$

1

(f) MOSFET has large input impedance

OR

MOSFET causes no loading of the logic gate output. ✓

1

[9]

3. (a)

Number shown on die	Logic inputs			Logic outputs						
	C	**B**	**A**	**L1**	**L2**	**L3**	**L4**	**L5**	**L6**	**L7**
1	0	0	0	0	0	0	0	0	0	1
2	0	0	1	1	0	0	0	0	1	0
3	0	1	0	1	0	0	0	0	1	1
4	0	1	1	1	0	1	1	0	1	0
5	1	0	0	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1	1	1	0
Reset 6 → 1										

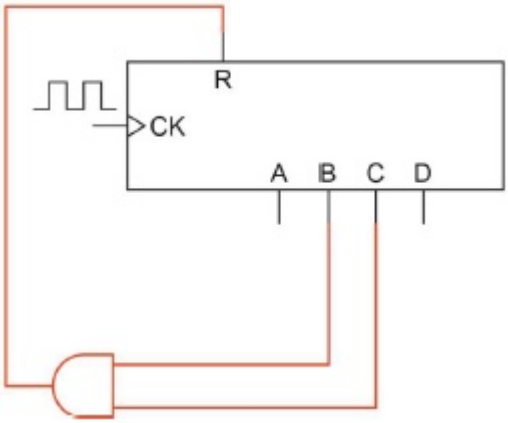
*One mark for each full pattern of **L1** and **L6:***

2

(b) **L7 = NOT A;** Accept: L7 = $\overline{A}$

1

(c)



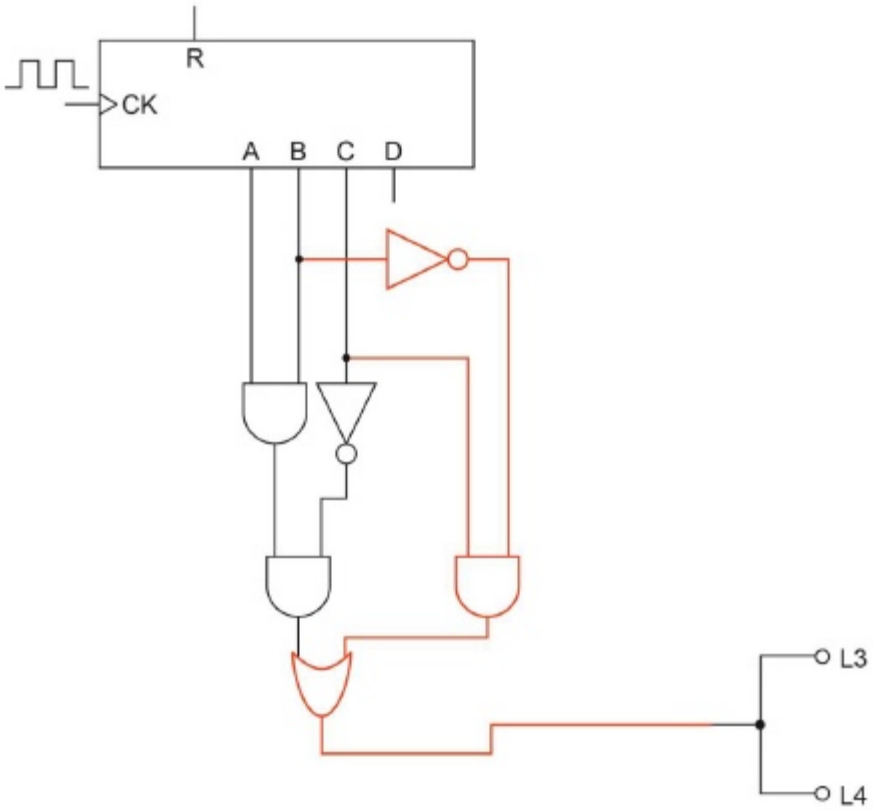
1 mark for reset condition from B and C

1 mark for use of a single 2-input AND gate

(accept correct implementation of the full reset code $\overline{A}$.B.C for 1 mark)

2

(d)



1 mark - NOT gate from B:

1 mark - AND gate from $\overline{B}$ and C:

1 mark - OR gate connecting the two conditions:

3

[8]

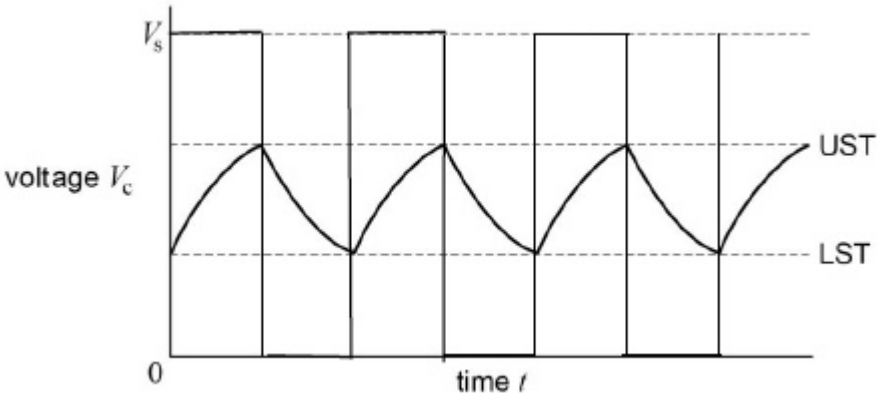
4. (a) PRF = 1 / (1.4 RC)

= 1 / ($1.4 \times 5.1 \times 10^3 \times 10 \times 10^{-9}$)

14 kHz ✓

1

(b) Square wave with correct phase and amplitude ✓



1

(c) New resistor calculated and stated to be 1.7 kΩ ✓

New resistor placed in parallel with original resistor ✓

Ecf from part (a)

2

(d) $T = \frac{1}{f} = \frac{1}{5 \times 10^3}$ = 0.2 ms (200 µs)

$t_C = 0.2 \times 10^{-3} \times \frac{3}{4}$ = 150 µs

$t_D = 0.2 \times 10^{-3} \times \frac{1}{4}$ = 50 µs

$R_2 = \frac{t_D}{0.7 \times C} = \frac{50 \times 10^{-6}}{0.7 \times 10 \times 10^{-9}}$ = 7.1 kΩ (Accept 7kΩ)

$R_1 = \frac{t_C}{0.7 \times C}$ – R2 = 14.3 kΩ (Accept 14kΩ)

1 mark for significant calculation
Eg showing $R_1 = 2R_2$
OR
Calculation for t_C or t_D
1 mark for values of R_1 and R_2

2

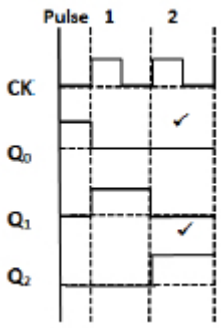
(e) Two properties per mark – (max mark 2)✓✓

- A square wave
- Amplitude of 0 V to 5 V
- Periodic time of 0.2 ms
- High for 0.15 ms – Low for 0.05 ms

2

[8]

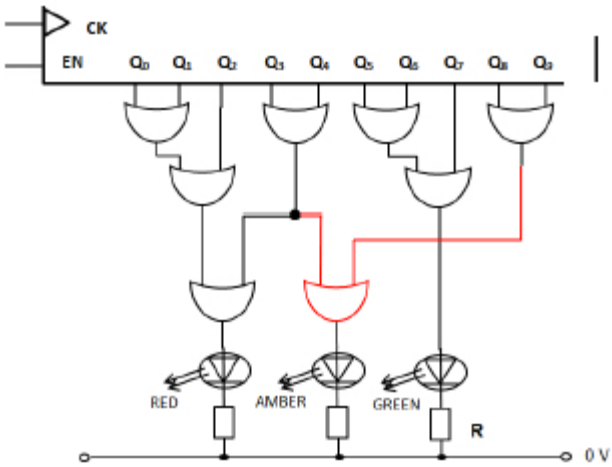
5. (a)



Flat line of Q_0 - 1 mark
Correct fall of Q_1 and rise of Q_2 - 1 mark

2

(b)



Logic OR gate correctly connected in position for 1 mark

1

(c) The ON time for the green LED is determined by:

the frequency of the clock ✓

the number of adjacent outputs that are OR'ed ✓

Accept reference to the period of the clock pulse.

2

(d) **R** = V_R / I ; **R** = (9 – 2.1) V ✓ / 9 mA

R = 6.9 V / 9 mA ; **R** = 767 Ω ✓

Minimum resistor value that can be used in order not to exceed 9 mA is 767 Ω.

The 720 Ω resistor range is (684 to 756) Ω and falls below this value so should not be used. ✓

OR

Calculation using 720 Ω ±5% Resistor range = (684 to 756) Ω ✓ leading to smallest current of 9.1 mA ✓

This current will exceed the permitted value of 9 mA. Don't use. ✓

$_1$One mark for voltage across the resistor

$_2$One mark for a suitable I-V-R calculation

$_3$One mark for conclusion with reason.

Use of error range to give max resistance must be seen in either $_2$ or $_3$ for that mark to be awarded.

3

[8]

6. (a) Q = ($\overline{A}$.B) + (A.$\overline{B}$) ✓✓ (allow written format)
Do not allow (A ⊕ B)

- *Correct two terms* ✓
- *Correct operator for OR gate* ✓

2

(b)

B	A	C	D	E	F	Q
0	0	1	1	0	0	0
0	1	0	1	0	1	1
1	0	1	0	1	0	1
1	1	0	0	0	0	0
		✓		✓		

Correct column C
Correct column E

2

(c) Any two criteria ✓✓

Less complex circuit – easier to manufacture
Only uses one type of chip – more economical to buy
Uses fewer ICs so saves space
Uses fewer ICs so saves on power consumption
Accept any other valid reason

2

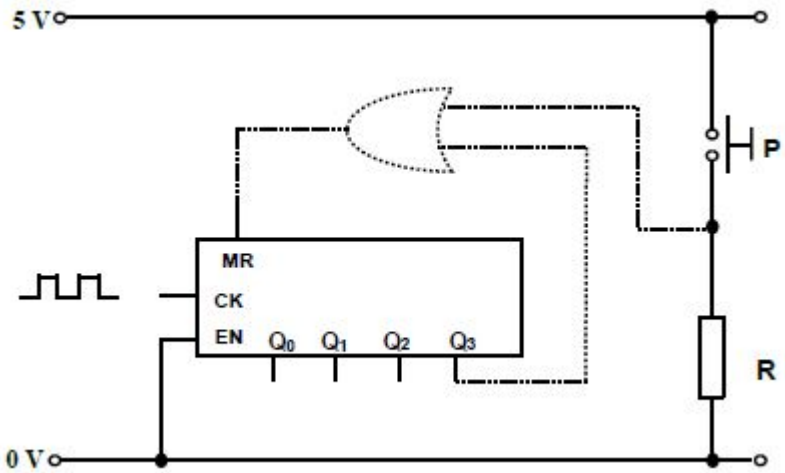
(d) EOR ✓
Also allow EXOR, XOR

1

[7]

7.

(a)



Correct logic gate to MR ✓
Q_3 to logic gate input ✓
Midpoint of switch chain to logic gate input ✓

OR

Accept 2 diodes in correct position ✓✓ Correct orientation ✓

2 marks only for both resets in correct positions but no logic gate.
1 mark only for any correct single reset circuit.

3

(b) **(A . C)** ✓ + **(B . $\overline{C}$)** ✓

Second mark includes the (+)
Also allow commutative equivalents such as ***(B. $\overline{C}$) + (A.C)***

2

(c)

Decimal number	C	B	A	D	E	F	W
0	0	0	0	1	0	0	0
1	0	0	1	1	0	0	0
2	0	1	0	1	0	1	1
3	0	1	1	1	0	1	1
4	1	0	0	0	0	0	0
5	1	0	1	0	1	0	1
6	1	1	0	0	0	0	0
7	1	1	1	0	1	0	1

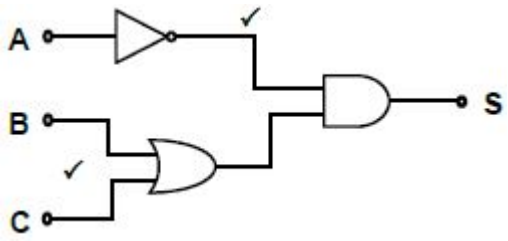
1

(d) numbers 2, 4 and 6 ✓

accept even numbers

1

(e)



NOT A into the AND gate ✓

(B OR C) into the AND gate ✓

Only 1 mark if AND gate is incorrect

Do not accept use of NAND, NOR, EXOR / EXNOR gates to generate equivalent functions.

2

[9]

8. (a) Difference: BCD counter outputs binary codes. A Johnson decade counter outputs a single output sequentially✓

Similarity: Both counters recycle at the 10th pulse ✓

Both outputs described.

Condone – max counter value for 10th pulse.

Accept: both counters count from 0–9

OR both counters count to 10

2

(b) Duty cycle:

From oscilloscope t_{on} = 3 div @ 50 µs / div = 150 µs
OR
t_{off} = 2 div @ 50 µs / div = 100 µs ✓

$\frac{t_{on}}{(t_{on} + t_{off})} \times 100 = 60\%$ OR 0.6 ✓

(accept 'divisions' to signify the values of t_{on} and t_{off})

Frequency:

From CRO t_p = 5 div @ 50 µs / div
t_p = 250 µs

$f = 1/t_p$ = 4 kHz ✓

Only 1 mark for:

either of t_{on} or t_{off} correct but duty cycle wrong

OR

correct use of both wrong t_{on} and t_{off}

One mark for:

correct use of their t_{on} + t_{off}

3

(c) **BCD:** Q_2 = 600 / 10 = 60 Hz ✓

(only one pulse is produced in 10 clock pulses at Q_2)

Johnson: Q_2 = 600 / 10 = 60 Hz ✓

2

[7]