Unit 8: Boolean Algebra
(AS Content)

Marks: /13

Answer **all** the questions.

1. Draw the logic gates represented by the Karnaugh Map below. Show your working.

CD \ AB	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	1	1
10	0	0	1	1

[4]

2. An electronics engineer needs a circuit with the following logic.

$(A \wedge B) \vee (\neg A \wedge B) \vee (\neg C \wedge \neg D)$

Complete and use the Karnaugh map below to simplify the expression above.

CD \ AB	00	01	11	10
00				
01				
11				
10				

Simplified expression:

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[4]

3(a).

Draw an XOR gate.

[1]

(b). Explain the difference in the function of OR and XOR gates.

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[2]

4. A NAND gate and its truth table are shown in Fig. 10.1.

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

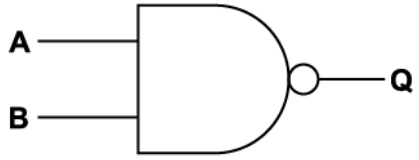
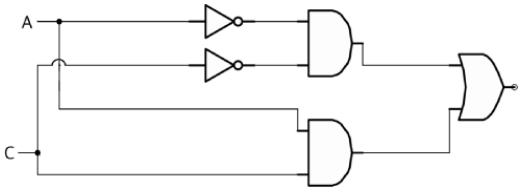


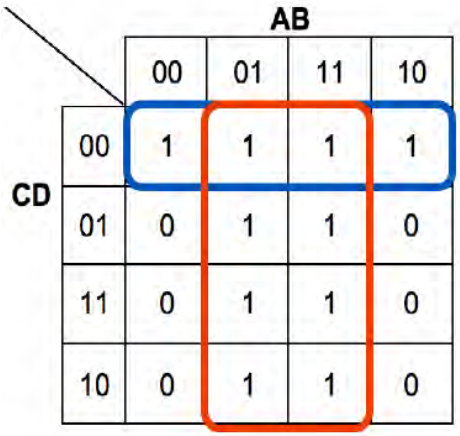
Fig. 10.1

Draw a set of gates equivalent to a NAND gate, but built only of AND, OR and NOT gates.

[2]

END OF QUESTION PAPER

Question			Answer/Indicative content	Marks	Guidance
1			– Correctly identified groups on Karnaugh map / Correct boolean statement.(1) – NOT A AND NOT C Gates (1) – A AND C gates (1) – Both sets of gates joined by OR gate (with no other gates used). (1)	4 (AO2.2)	AB CD 00 01 11 10 00 1 1 0 0 01 1 1 0 0 11 0 0 1 1 10 0 0 1 1 (¬A ∧ ¬C) ∨ (A∧C) Or equivalent.  Or equivalent. **Examiner's Comments** Most candidates scored well on these questions demonstrating their understanding of logic gate circuits. Some candidates simplified the circuit in part b) which achieved full marks provided the resultant circuit gave the same output.
			Total	4	

Question			Answer/Indicative content	Marks	Guidance
2			Simplified expression: B v (¬C∧¬D)  	4	For 4 marks. 1 mark for simplified expression: B ∨ (¬C∧¬D) 1 mark for filling in table correctly. 1 mark for identifying each grouping (maximum 2). Allow follow through if tabled filled incorrectly giving one mark for each valid grouping if it is the most efficient possible to a maximum of two marks.
			Total	4	
3	a			1 AO1.1	Accept diagram of gate only without input / output **Examiner's Comment** There were very few candidates who could not correctly draw an XOR gate.
	b		OR gate outputs true if at least one of its inputs is true (1) XOR gate output true if and only if one of its inputs is true. (1)	2 AO1.2	Accept appropriate, correctly labelled, truth tables. One mark for each truth table. **Examiner's Comment** A lack of clarity of expression led to candidates not gaining credit in this question. Some candidates who achieved full marks supported their descriptions with correct two-input truth tables which clearly demonstrated the difference.
			Total	3	

Question			Answer/Indicative content	Marks	Guidance
4			 One AND one NOT gate used (1) In correct configuration (1)	2	
			Total	2	