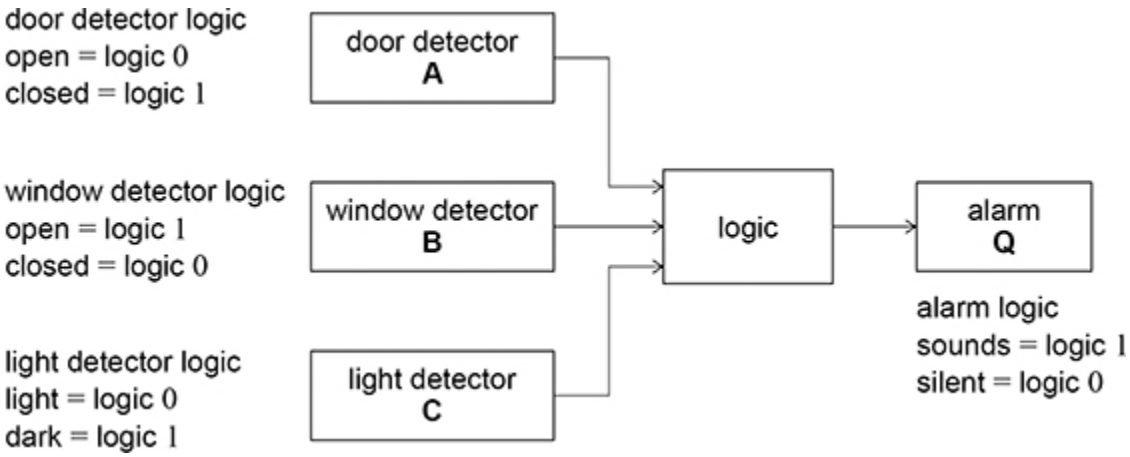
1. A burglar-alarm system in a house sounds an alarm during the hours of darkness when **one** of the following conditions is met:

- the door is opened
- the window is opened
- both the door and the window are opened.

Figure 1 shows the main burglar-alarm subsystems and the logic status for the inputs and output.

Figure 1



(a) The table below is a partially completed truth table for the logic subsystem.

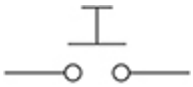
Inputs			Output
C	**B**	**A**	**Q**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	
1	1	0	
1	1	1	

Complete the table above.

(1)

Figure 2 shows the symbol of the push-to-make switch used in the door detector. When the door is closed, the switch button is pushed down onto the contacts. It automatically releases when the door opens.

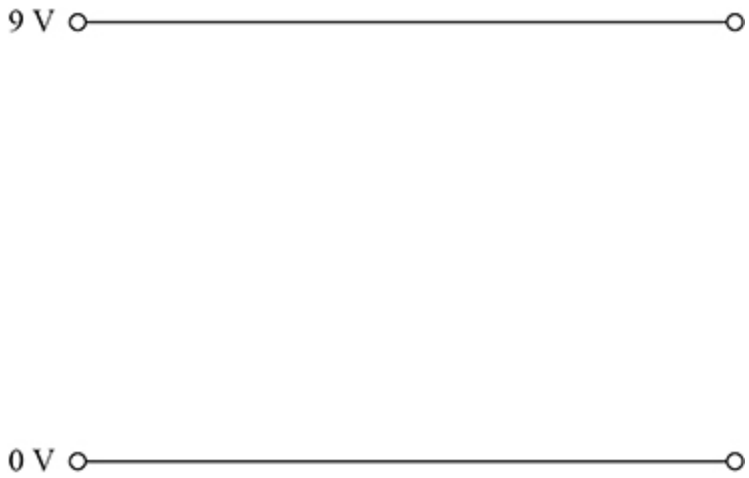
Figure 2



(b) Complete **Figure 3** to show how this switch, together with a 10 kΩ resistor, can be connected to create the door detector circuit in **Figure 1**.

Label the output of the circuit with an **X**.

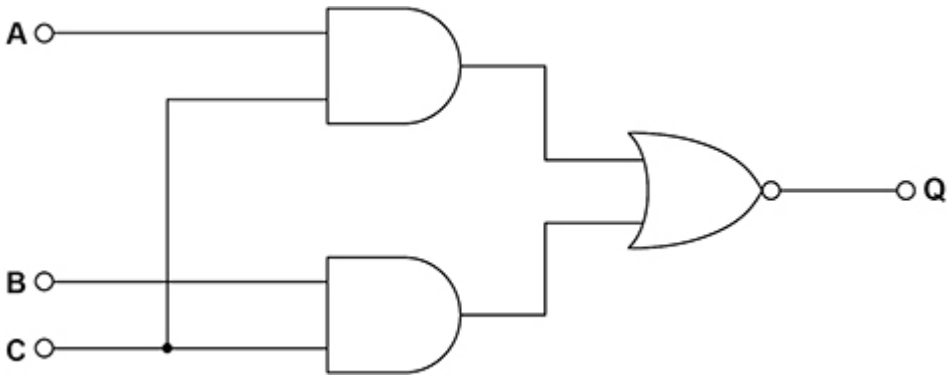
Figure 3



(2)

Figure 4 shows a logic circuit for a different alarm system.

Figure 4



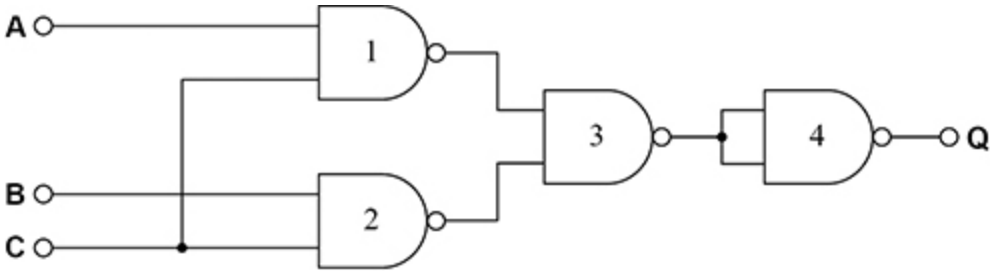
(c) Write the Boolean algebra expression for **Q** in terms of inputs **A**, **B** and **C**.
In your answer use only AND and NOR operators.

Q = _____

(2)

(d) **Figure 5** shows a logic circuit that has the same function as the circuit in **Figure 4**. Only one type of gate is used in the circuit in **Figure 5**.

Figure 5



State the logic function performed by gate 4.

_____

(1)

(e) Microchips containing two-input logic gates are mass-produced. Each microchip contains four identical logic gates.

A manufacturer of the logic circuit used in the burglar alarm chooses to make the circuit in **Figure 5** rather than that in **Figure 4**.

Suggest why.

_____

_____

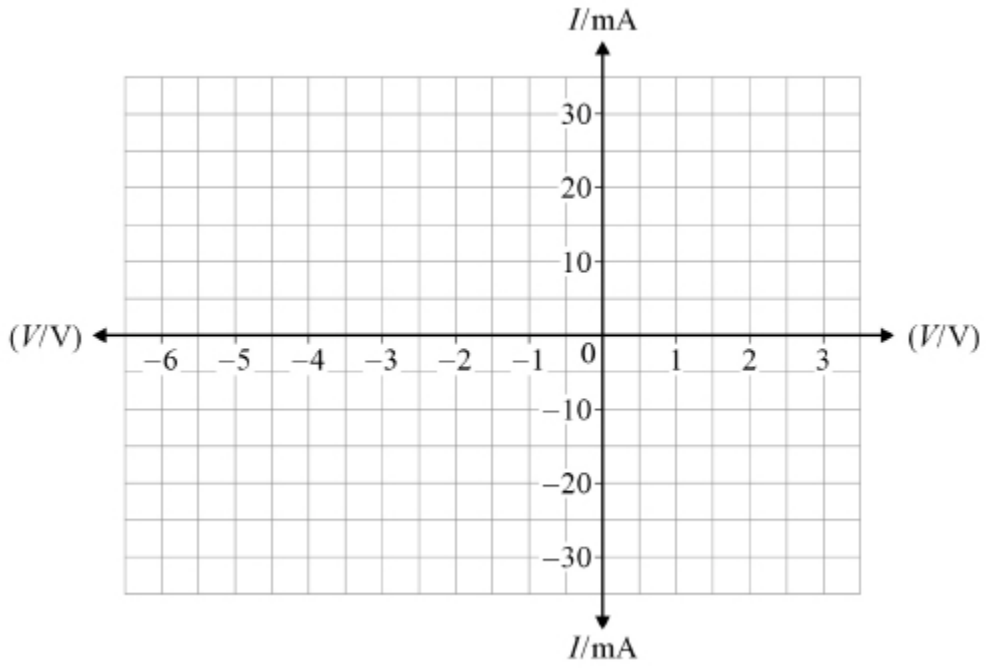
(1)

(Total 7 marks)

2. A silicon-based 5.1 V Zener diode requires a minimum operating current I of 5.0 mA to maintain its Zener voltage V_z.

(a) Draw on **Figure 1** the general $I-V$ characteristic for this diode.

Figure 1

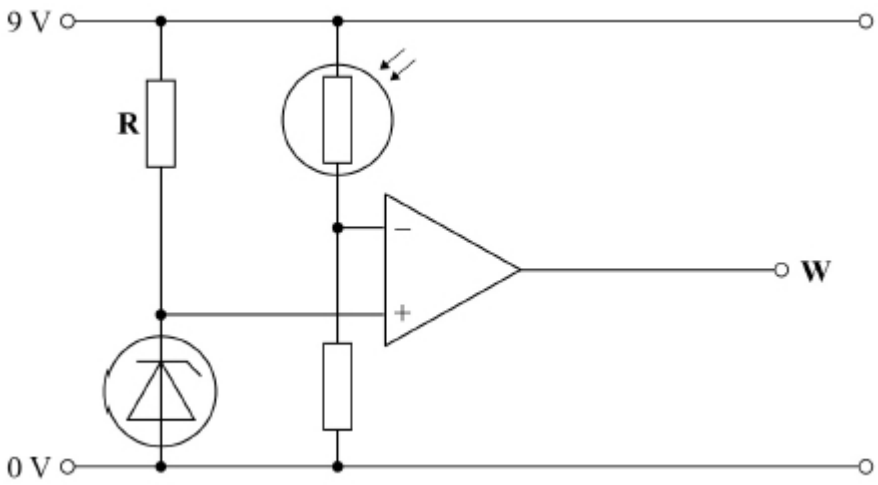


(2)

(b) **Figure 2** shows a circuit that uses a 5.1 V Zener diode.

The circuit causes the output **W** of the operational amplifier to change at a particular light intensity.

Figure 2



State the function of the Zener diode in this circuit.

_____

(1)

(c) Deduce whether a 100 Ω, 0.13 **W** resistor is suitable for **R** in **Figure 2**.

_____

_____

_____

_____

(2)

(d) The circuit in **Figure 2** is rebuilt and the position of **R** is swapped with the position of the Zener diode.

Explain how this affects the light intensity at which **W** changes.

_____

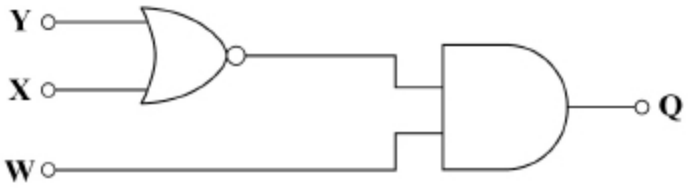
_____

_____

(2)

(e) The output **W** from the operational amplifier shown in **Figure 2** becomes one of three inputs to the combinational logic circuit shown in **Figure 3**.

Figure 3



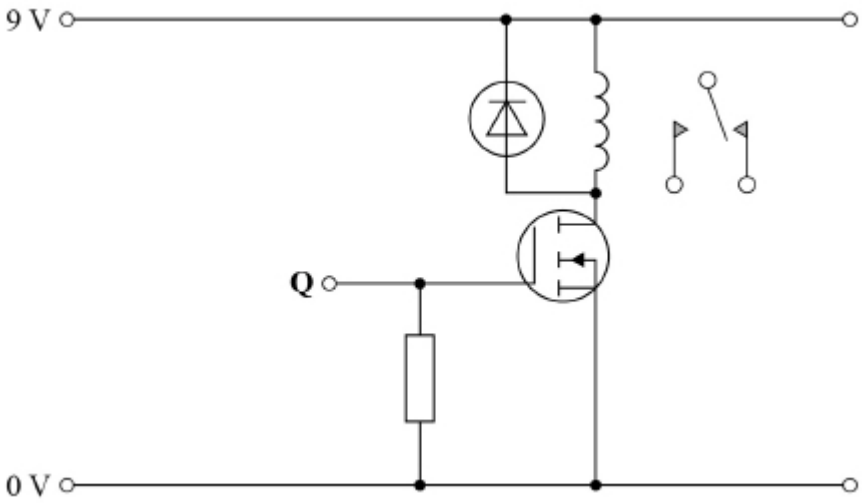
Write the Boolean algebra expression for the output **Q** in terms of **W**, **X** and **Y** based on the logic gates shown in **Figure 3**.

Q = _____

(1)

(f) Output **Q** from **Figure 3** becomes the input to the final part of the circuit shown in **Figure 4**.

Figure 4



The circuit uses a MOSFET to activate a relay.

State **one** property that makes the MOSFET suitable for interfacing with logic gates.

_____

(1)

(Total 9 marks)

3. A die, where dots on the faces of a cube indicate the numbers 1 to 6, is shown in **Figure 1** and is used in many games.

Figure 1

A student makes an electronic version of this by feeding pulses from a pulse generator into a 4-bit binary counter.

The circuit uses the first three outputs of the counter A (least significant bit), B and C.

By feeding the outputs from the counter through logic gates, the seven LEDs shown in **Figure 2** can be made to display the numbers 1 to 6 in sequence.

Figure 2

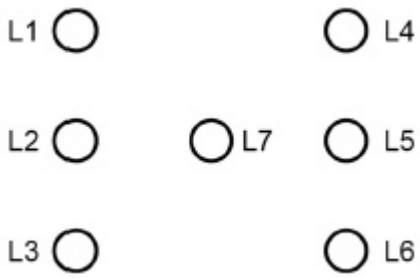
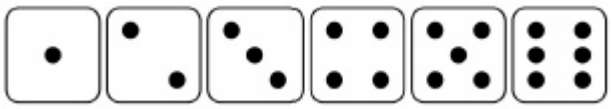


Figure 3 shows the sequence of numbers.

Figure 3



The black dots show which LEDs are lit for each of the numbers 1 to 6.

The partially completed truth table below shows which of the LEDs (L1 to L6) are ON (logic 1) and which are OFF (logic 0) during the counting sequence.

Number shown on die	Logic inputs			Logic outputs						
	C	B	A	L1	L2	L3	L4	L5	L6	L7
1	0	0	0		0	0	0	0		1
2	0	0	1		0	0	0	0		0
3	0	1	0		0	0	0	0		1
4	0	1	1		0	1	1	0		0
5	1	0	0		0	1	1	0		1
6	1	0	1		1	1	1	1		0
Reset 6 → 1										

(a) Complete the table to show the logic outputs for the lamps L1 and L6.

(2)

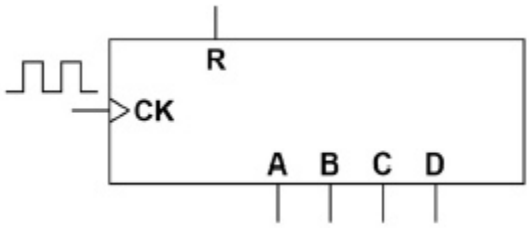
(b) Deduce the **simplest** Boolean expression that can be used to show how output L7 can be controlled by the logic inputs.

_____

(1)

(c) **Figure 4** shows some of the input and output pins of the 4-bit binary counter.

Figure 4



The data sheet for the counter indicates that the counter resets when the reset pin **R** is taken from logic 0 to logic 1.

Draw on **Figure 4** the logic gate needed and the connections required from the outputs to the reset pin **R** on the counter so that the counter cycles as required.

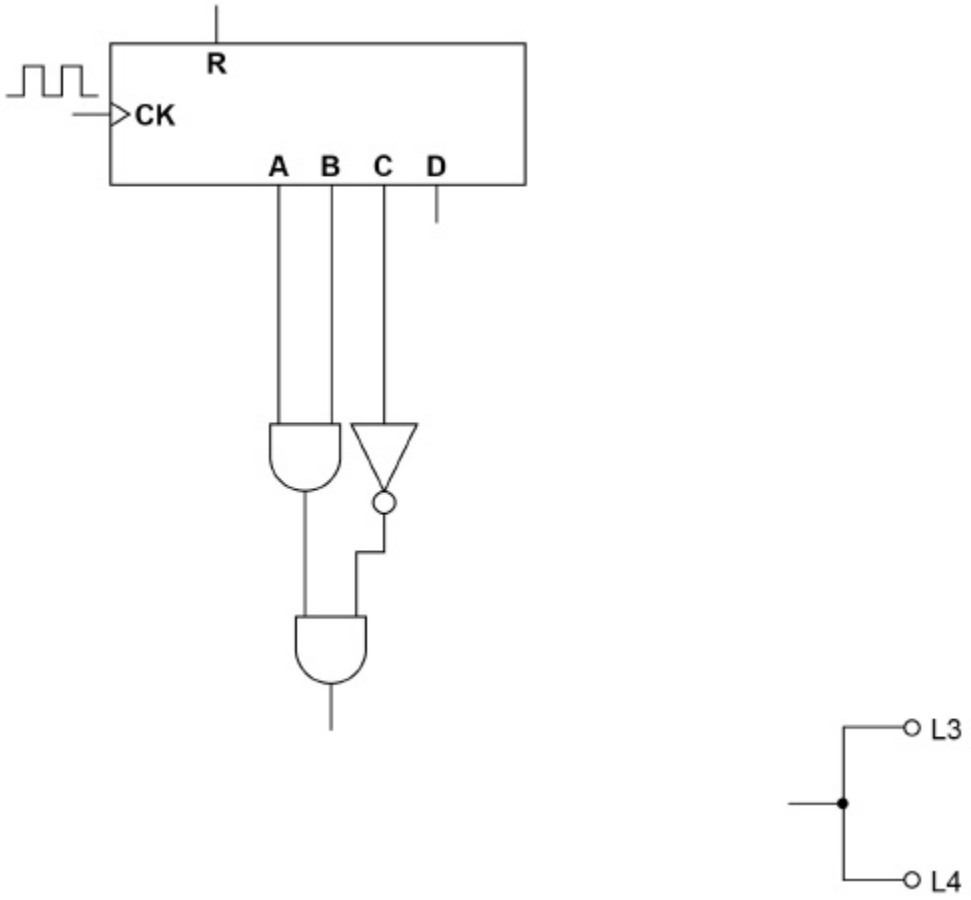
(2)

(d) The output of both L3 and L4 can be written as **(A.B.$\overline{C}$) + ($\overline{B}$.C)**

Figure 5 shows part of a logic circuit needed to represent this Boolean expression.

Complete the logic circuit in **Figure 5** by adding AND, OR and NOT gates.

Figure 5

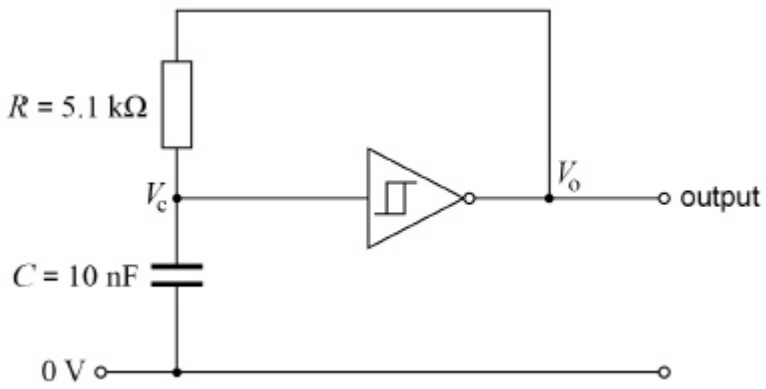


(3)

(Total 8 marks)

4. (a) **Figure 1** shows an astable circuit based on a NOT logic gate. The symbol in the centre of the logic gate means that the output V_o changes at two different input values of V_c depending on whether the input voltage is rising or falling.

Figure 1



The pulse repetition frequency (PRF) for this particular circuit is given by:

$$\frac{1}{1.4\,RC}$$

Calculate the PRF in kHz

PRF = _____ kHz

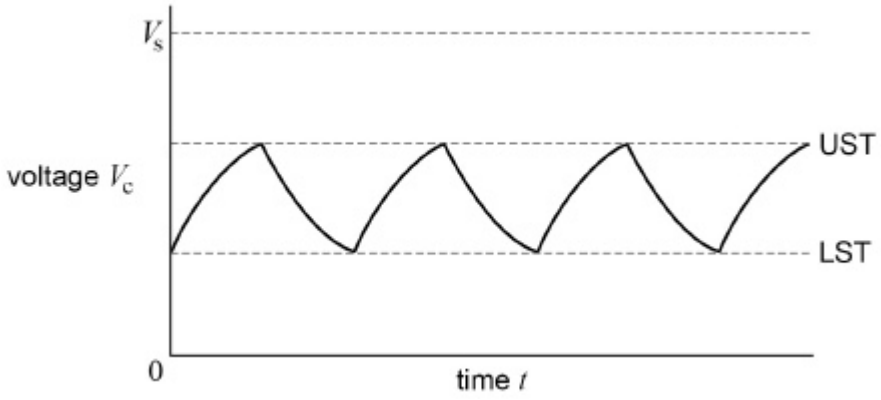
(1)

(b) The supply voltage to the NOT gate is V_s

- When V_c increases and reaches the upper switching threshold (UST), the output of the NOT gate will switch from V_s to 0 V
- When V_c decreases and reaches the lower switching threshold (LST), the output of the NOT gate will switch from 0 V to V_s

The graph in **Figure 2** shows V_c constantly changing as the capacitor charges and discharges.

Figure 2



Draw on **Figure 2** the output voltage V_o for the astable circuit.

(1)

(c) The circuit in **Figure 1** can be modified by the addition of a resistor to vary the PRF.

The astable is to be modified so that it produces a frequency 4 times that of the original.

Calculate the value of the resistor that should be added to the circuit and explain where in the circuit this additional resistor should be placed.

value of resistor = _____ kΩ

_____

_____

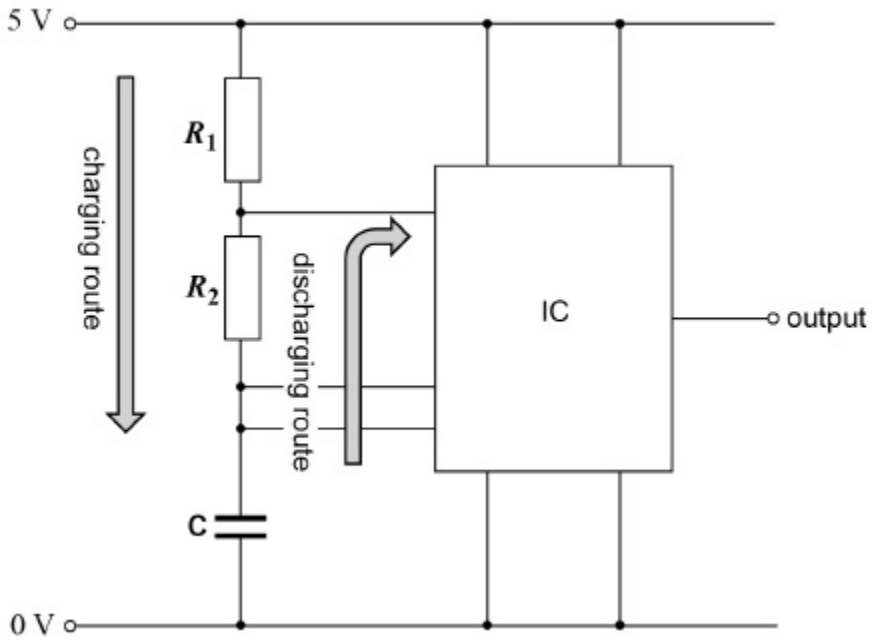
_____

_____

(2)

(d) In another astable, two resistors (R_1 and R_2) and a capacitor **C** form a timing chain to control the mark and space times for a square wave produced at the output of the integrated circuit (IC) shown in **Figure 3**.

Figure 3



The charging time for the capacitor **C** is: $t_C = 0.7 \times (R_1 + R_2) \times C$

The discharging time for the capacitor **C** is: $t_D = 0.7 \times R_2 \times C$

Calculate, in kΩ, values for $\boldsymbol{R_1}$ and $\boldsymbol{R_2}$ needed to produce a 5 kHz signal with 75% duty cycle given that the capacitor **C** has a value of 10 nF

$\boldsymbol{R_1}$ = _____ kΩ

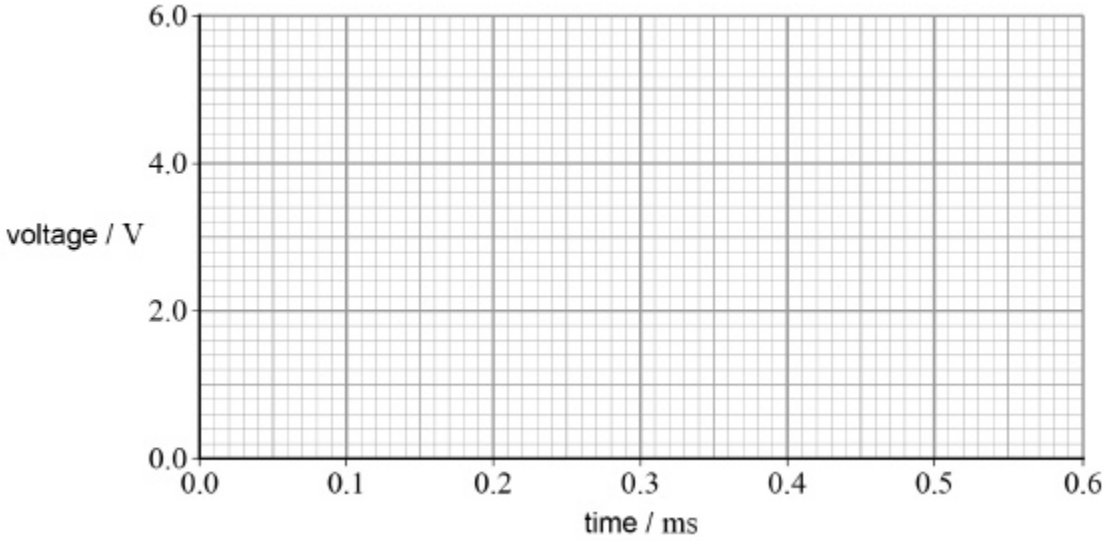
$\boldsymbol{R_2}$ = _____ kΩ

(2)

(e) The output of the IC in **Figure 3** is 5 V during the charging period and 0 V during the discharging period.

Draw on **Figure 4** the wave pattern that represents this signal.

Figure 4

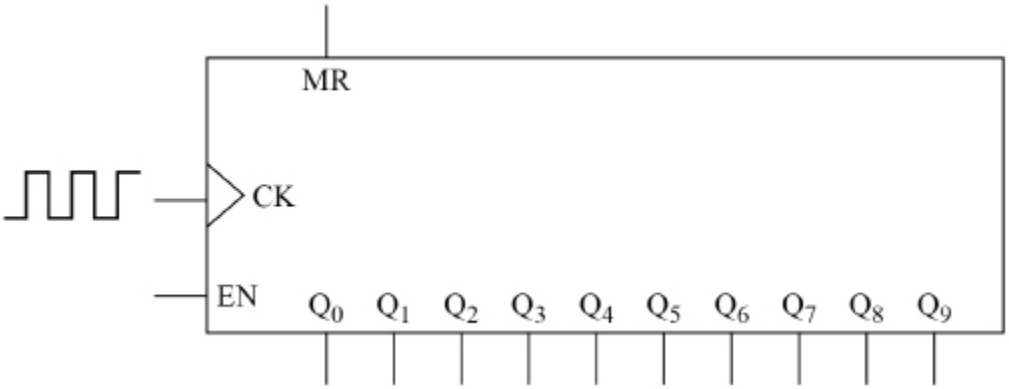


(2)

(Total 8 marks)

5. **Figure 1** shows the basic layout for a Johnson decade counter.
The main input is the clock (CK).
The main outputs are shown as Q_0 to Q_9.

Figure 1

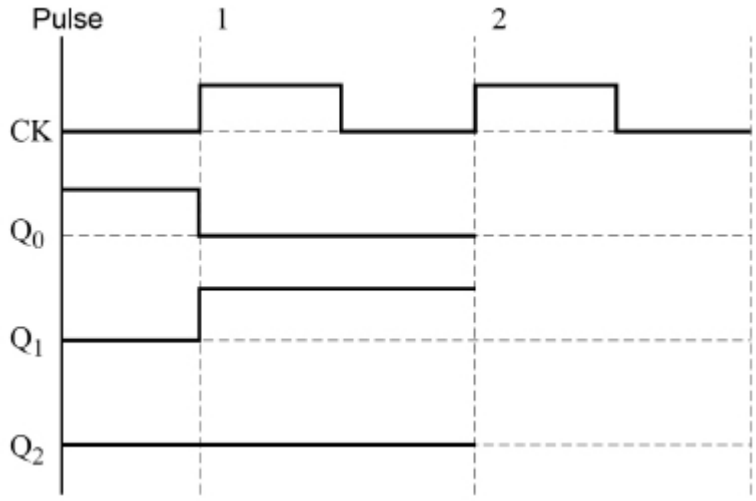


(a) **Figure 2** shows part of the timing diagram for a Johnson decade counter.

This timing diagram shows the output logic states against time. The counter is reset to make $Q_0 = 1$ and then the first two pulses are applied.

Complete **Figure 2** to show the logic states of Q_0, Q_1 and Q_2.

Figure 2



(2)

(b) A student sets up the counter to make the traffic light sequence:

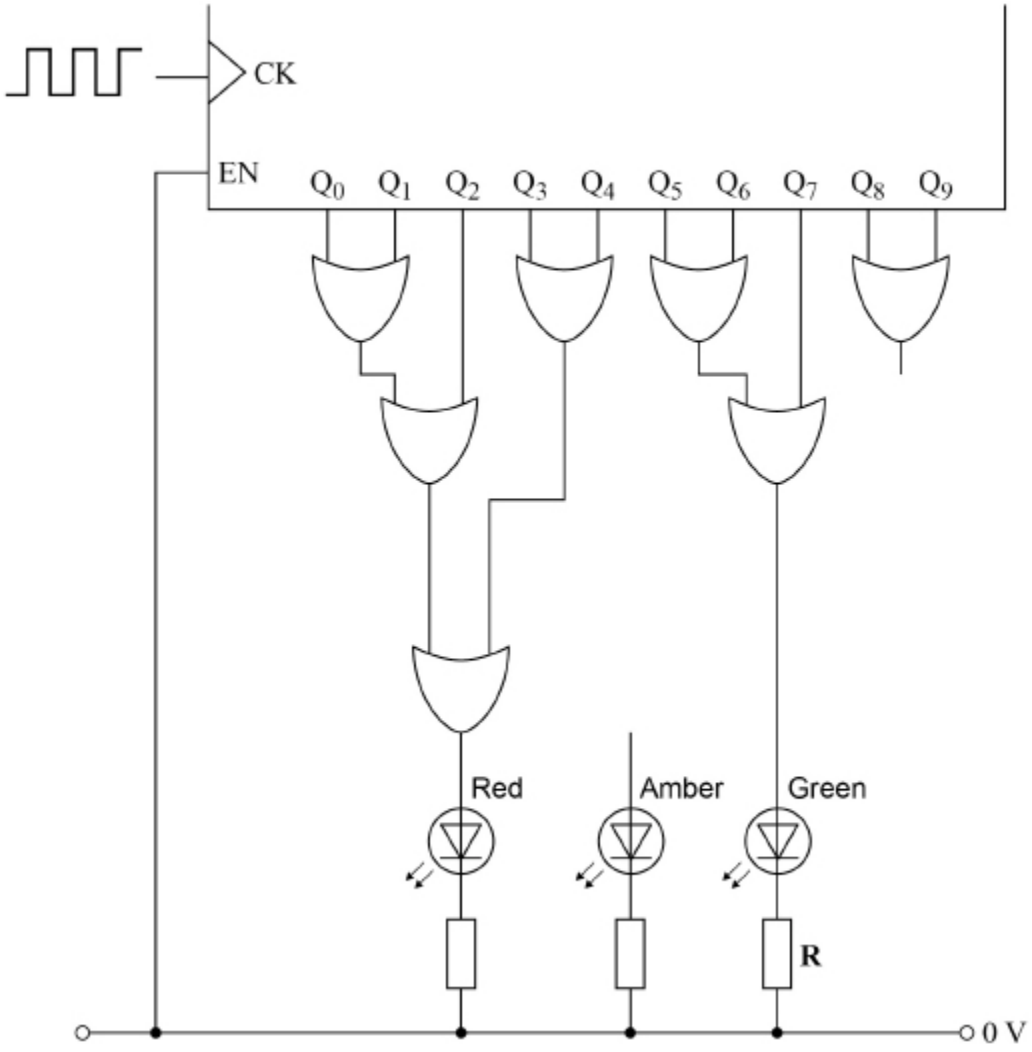
red → red + amber → green → amber

The sequence then repeats.

Figure 3 shows a partially completed diagram for producing this sequence.

Draw an OR gate and connections on **Figure 3** so that the LEDs go through the complete sequence.

Figure 3



(1)

(c) State **two** factors that determine the ON time for the green LED shown in **Figure 3**.

1 _____

_____

2 _____

_____

(2)

(d) The potential difference across the green LED is 2.1 V when it is lit. The current through it should not exceed 9 mA.

All logic gate outputs are:
logic low = 0 V
logic high = 9 V.

The student suggests that a resistor of resistance 720 Ω and a tolerance of ±5% should be used for **R**.

Deduce whether the student's suggestion would be suitable.

_____

_____

_____

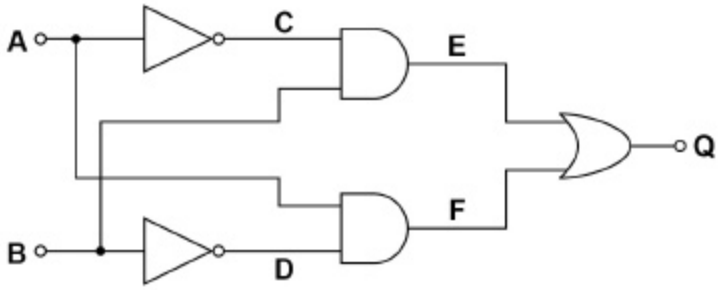
_____

(3)

(Total 8 marks)

6. (a) Two logic inputs, **A** and **B**, feed into the logic circuit shown in **Figure 1**. The logic output from the circuit is **Q**.

Figure 1



Deduce the Boolean expression for the output of this logic circuit in terms of inputs **A** and **B**.
Include all the logic operations that take place between the inputs and the output.

Q = _____

(2)

(b) The truth table shows some of the logic states for the logic gates in **Figure 1**.

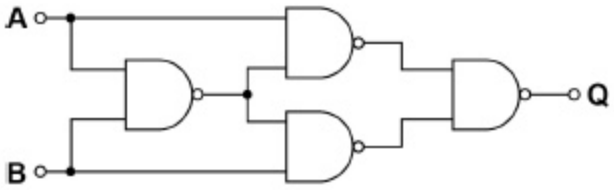
Complete the truth table.

B	A	C	D	E	F	Q
0	0		1		0	0
0	1		1		1	1
1	0		0		0	1
1	1		0		0	0

(2)

(c) **Figure 2** shows a different logic circuit that produces the same logic output as that of **Figure 1**.

Figure 2



A manufacturer wants to produce a system that uses this logic function, but is undecided as to which circuit to use.

Suggest, giving reasons, **two** benefits of using the logic circuit in **Figure 2** compared to the logic circuit in **Figure 1**.

_____

_____

_____

_____

_____

_____

(2)

(d) State the single logic gate that would perform the same logic function as the circuits shown in **Figure 1** and **Figure 2**.

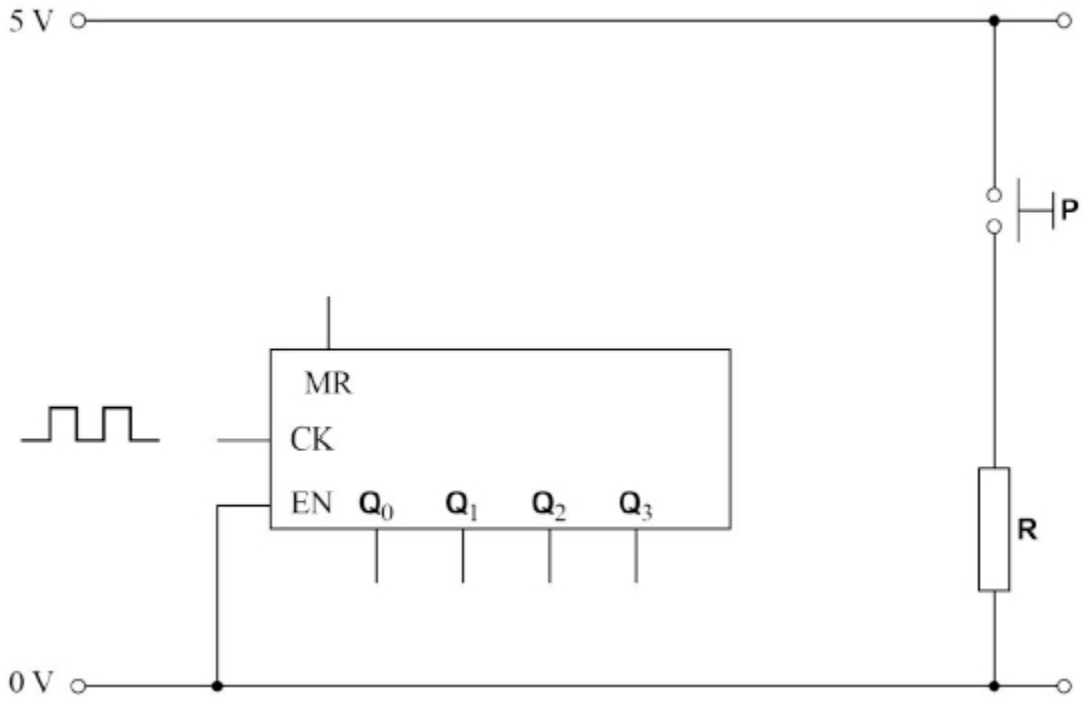
_____

(1)

(Total 7 marks)

7. **Figure 1** shows part of a circuit that includes a 4-bit binary counter. The main inputs and outputs of the counter are shown.
The counter generates a sequence of binary codes representing the decimal numbers 0 to 7
Output $\mathbf{Q_0}$ is the least significant bit of the binary codes.

Figure 1



The counter resets when the master reset pin MR receives a logic 1

The circuit requires the counter to reset when either one of two conditions is met.

Condition 1 Manual reset using the switch **P** to reset the counter to 0

Condition 2 Automatic reset when an appropriate binary code is produced at the counter outputs. This will cause the counter to continually cycle through the decimal numbers 0 to 7

(a) Complete **Figure 1** to show how both reset conditions can be met.

Do **not** show the power line connections to the integrated circuit.

(3)

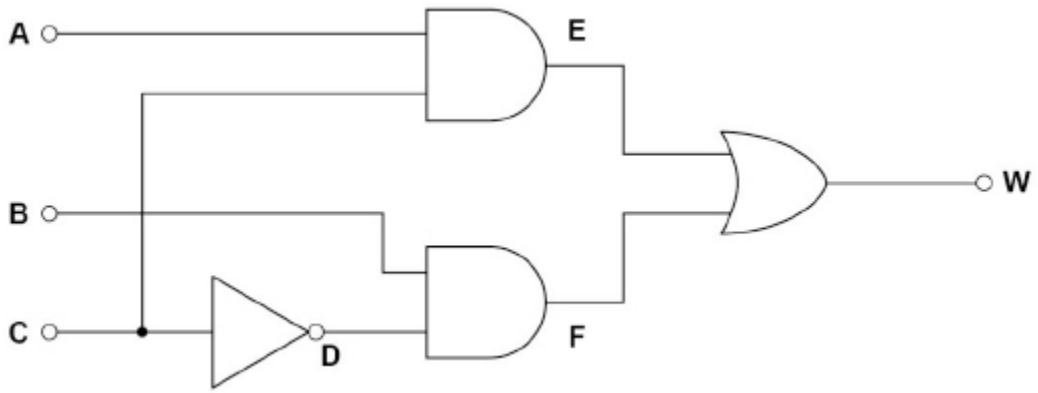
(b) A logic system is designed to identify prime numbers.

The binary codes from the counter are now applied to the inputs **ABC** of the logic system shown in **Figure 2**.

Input **A** takes the least significant bit of the binary code from the counter.

Output **W** becomes logic state 1 when a prime number 2, 3, 5 or 7 is detected. Otherwise output **W** is at logic 0

Figure 2



Write the Boolean algebra expression for output **W** in terms of the inputs **A**, **B** and **C**. The expression must contain only the four logic gate operations shown in **Figure 2**.

W= _____

(2)

(c) Complete the truth table for the logic system in **Figure 2**.

Decimal number	C	B	A	D	E	F	W
0	0	0	0	1	0		0
1	0	0	1	1	0		0
2	0	1	0	1	0		1
3	0	1	1	1	0		1
4	1	0	0	0	0		0
5	1	0	1	0	1		1
6	1	1	0	0	0		0
7	1	1	1	0	1		1

(1)

(d) The logic system in part (b) is replaced with one that gives an output **S** using the same binary input codes **CBA**.

The Boolean algebra equation for output **S** is

$$\mathbf{S} = \overline{\mathbf{A}} . (\mathbf{B} + \mathbf{C})$$

Deduce which decimal numbers 0 to 7 will cause **S** to become logic 1

(1)

(e) Complete **Figure 3** by drawing the logic system for **S**.

You must use only the logic gate operations given in $S = \overline{A}.(B + C)$

Figure 3

(2)

(Total 9 marks)

8. A Johnson decade counter uses a Johnson counter together with decoding logic. This arrangement produces a single logic 1 at a series of outputs Q_0–Q_9 in a continuous sequence.

(a) Describe **one** functional difference and **one** functional similarity between how a Johnson decade counter and a BCD counter output their counts.

functional difference _____

_____

_____

_____

functional similarity _____

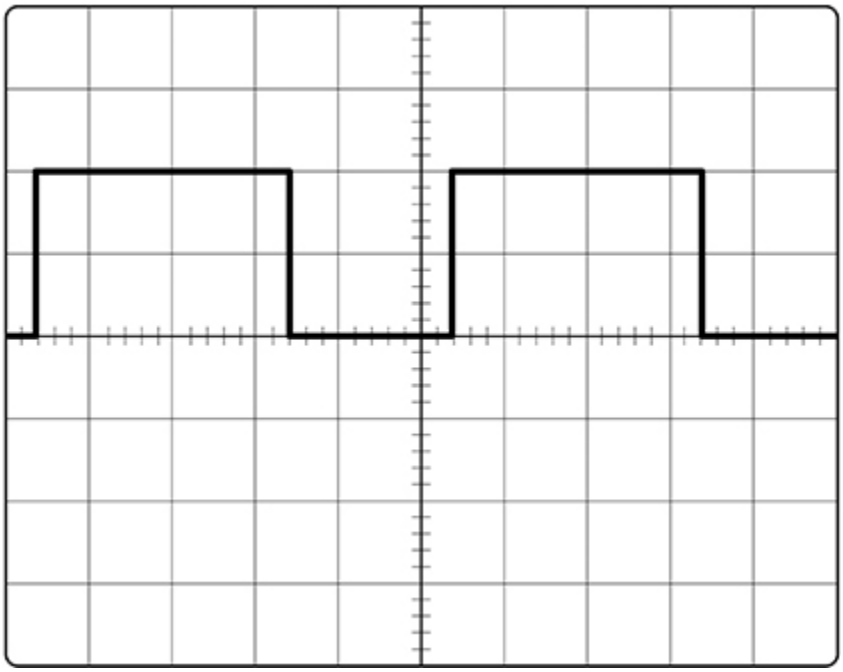
_____

_____

_____

(2)

(b) An astable oscillator produces a continuous train of pulses.
The figure below shows the display of the pulses on an oscilloscope.



The oscilloscope settings are:

voltage gain = 2 V / division
time-base = 50 μs / division.

Determine the duty cycle and frequency of the signal.

duty cycle = _____

frequency = _____ kHz

(3)

(c) The astable is adjusted to produce a 600 Hz test signal.

This signal is applied to the clock input of the BCD counter and to the clock input of the Johnson decade counter.

The outputs of the BCD counter are Q_0, Q_1, Q_2 and Q_3 where Q_0 is the least significant part of the output.
The outputs of the Johnson decade counter are Q_0, Q_1, Q_2 … Q_9.

Determine the frequency of the pulses available at Q_2 for each counter.

BCD counter: frequency of pulses = _____ Hz

Johnson decade counter: frequency of pulses = _____ Hz

(2)

(Total 7 marks)