Unit 1: Components of a Computer
(1b. Types of Processors, AS Content)

Marks: /20

Answer **all** the questions.

1(a).

(i) Compare a Complex Instruction Set Computer (CISC) architecture with a Reduced Instruction Set Computer (RISC) architecture.

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[4]

(ii) Explain **one** advantage, other than cost, of RISC compared with CISC.

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[2]

(b). Some computer systems use co-processors.

Explain the effect of using a co-processor system for each of the following applications.

(i) Complex calculations for scientific research.

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[2]

(ii) Printing personalised letters to customers for an advertising campaign.

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[2]

2. Von Neumann and array processor are different types of computer architecture.

One feature of Von Neumann architecture is that instructions are executed in a linear sequence.

(i) Give **three** other features.

1

2

3

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[3]

3(a). A computer uses a Von Neumann processor.

RISC and CISC are types of processor architecture.

Describe the differences between the **two** architectures.

[4]

(b). Describe the fetch-decode-execute cycle that this architecture uses.

Fetch

Decode

Execute

[3]

END OF QUESTION PAPER

Question			Answer/Indicative content	Marks	Guidance
1	a	i	*CISC:* Each instruction may take multiple cycles Single register set Instructions have variable format Many instructions are available Many addressing modes are available Complicated processor design Integrated circuit is expensive *RISC:* An instruction performs a simple task Limited number of instructions available Complex tasks can only be performed by combining multiple instructions Simple processor design	4	Max 3 marks for either CISC or RISC, total max 4 **Examiner's Comments** There were a wide variety of answers to this question, ranging from the very accurate to the very vague. A significant number of candidates said that RISC is used in mobile phones, if the question had asked for an example this would probably have been a good one. Those that missed marks here generally talked about the programming and its relative difficulty on either type of processor rather than the processor itself.
		ii	Programs run faster… …due to simpler instructions	2	**Examiner's Comments** Most candidates got the first mark, the more able candidates managed to get the second, again, here the most common erroneous answer was about the merits/drawbacks of programming.
	b	i	Calculations are done by the maths co-processor… …so processing is faster …when using floating point arithmetic	2	**Examiner's Comments** Both this and the next question were well answered by candidates who knew that a co-processor is for floating point calculations.
		ii	No increase in speed… …as co-processor not suitable for task / as there are no calculations	2	**Examiner's Comments** For this part there was a wide variety of inventions as to how a co-processor could control a print queue, not answered well by those who did not grasp the first part of the question.
			Total	**10**	

Question			Answer/Indicative content	Marks	Guidance
2		i	• Single control unit • One instruction at a time • Uses fetch execute cycle • Program & data stored together / program & data in same format	3	Accept single ALU Allow FDE Location TV **Examiner's Comments** A significant amount of candidates gave a single processor as a response to this question which was judged to not be sufficient for this level of examination.
			Total	3	
3	a		• CISC is more complex / RISC is simpler / CISC longer instruction set • RISC requires more RAM • CISC many address modes • CISC may have more registers • RISC takes one machine cycle / CISC takes many cycles to complete one instruction • RISC fixed number of bytes / CISC variable number	4	**Do not accept "task" in place of "instruction".** **Examiner's Comments** A fair number of responses were still mentioning cost as a difference: the Principal Examiner felt this response was not contextualised to computing and as such no credit was allowed for this.
	b		• Fetch- The next instruction is fetched from main memory/address • Decode- The instruction is interpreted / translated / split into opcode and operand (in the CIR) • Execute- The appropriate instruction/opcode is carried out on the operand.	3	**Fetch they may describe the whole cycle** **Not translated in MDR** **Examiner's Comments** A lot of candidates are unsure as to what actually happens in the fetch decode execute cycle and some very vague answers were provided. However, there were a few excellent responses that did show a good understanding of the processes.
			Total	7	

Question	Answer/Indicative content	Marks	Guidance